F0056.1663P PATENT

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	Zoran Krivokapic
Serial No.:	09/592,124
Filed:	June 12, 2000
Group Art Unit:	2823
Before the Examiner:	Pham, Long
Title:	METHOD AND SYSTEM FOR FORMING A LONG CHANNEL DEVICE

January 27, 2003

APPEAL BRIEF

Box AF
Assistant Commissioner for Patents
Washington, D.C. 20231

I. REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc., which is the assignee of the entire right, title and interest in the above-identified patent application.

CERTIFICATION UNDER 37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Box AF, Assistant Commissioner for Patents, Washington, D.C. 20231, on January 27, 2003

Signature

Kelly Kordzik

(Printed name of person certifying)

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant, Appellant's legal representative or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 9-16 are pending in the Application. Claims 9-16 stand rejected.

IV. STATUS OF AMENDMENTS

The Appellant's response to the Office Action having a mailing date of April 2, 2002, has been considered, but it does not place the application in condition for allowance because Appellant's arguments were deemed unpersuasive.

V. SUMMARY OF INVENTION

Semiconductor manufacturers have increasingly turned to high-density Metal Oxide Semiconductor (MOS) arrays in their integrated circuit design schemes. Specification, Page 1, Lines 6-7. To achieve a high-density integrated circuit, features such as metal-oxide semiconductor field-effect transistors (MOSFETs) must be as small as possible. Specification, Page 1, Lines 7-9. Integrated circuit device geometries well below one micron feature sizes continue to become increasingly common. Specification, Page 1, Lines 9-10.

Small geometry devices exhibit a severe short channel effect, which manifests as a rapid drop of threshold voltage with a decreasing channel length. Specification, Page 1, Lines 15-16. In order to prevent subsurface leakage between source and drain, which is not controlled by the gate bias, one has to increase the dopant concentration of the channel. Specification, Page 1, Lines 16-18. However, the increase in the dopant concentration of the channel severely reduces drive currents. Specification, Page 1, Lines 18-19. In order to

avoid this problem, a halo or pocket implant may be used since they do not increase the channel resistance but may be strategically placed to raise the potential barrier between the source and drain. Specification, Page 1, Lines 19-21.

Halo/pocket implants are moderately doped implants of the same conductivity type at the well or substrate in which the transistor is formed, and which lie in a thin layer generally along the source/drain to substrate/well junctions. Specification, Page 1, Line 22 - Page 2, Line 2. A combination of LDD structures and halo/pocket implants have proven to achieve good device performance and reliability. Specification, Page 2, Lines 2-3.

Although halo/pocket and LDD implants work well with digital applications, halo/pocket and LDD implants are not suitable for analog applications where the channel gate length exceeds .75 μm. Specification, Page 2, Lines 10-12. This is because long channel gates that have undergone halo/pocket and LDD implants have a significantly smaller Early Voltage which is undesirable for analog circuits. Specification, Page 2, Lines 12-14.

The problems outlined above may at least in part be solved in some embodiments by providing at least one active region on a substrate where the active region comprises a plurality of discontinuous gate structures. Specification, Page 4, Lines 2-4. An ion implantation may be provided in the substrate. Specification, Page 4, Lines 4-5. Consequently, a higher Early Voltage may be achieved enabling halo/implant and LDD implants to be effectively utilized in the design of analog circuitry. Specification, Page 4, Lines 6-8.

VI. ISSUES

A. Are claims 9-11 and 13-16 properly rejected under 35 U.S.C. §102(b) as being anticipated by Dennison et al. (U.S. Patent No. 6,004,854) (hereinafter "Dennison")?

B. Is claim 12 properly rejected under 35 U.S.C. §103(a) as being unpatentable over Dennison?

VII. GROUPING OF CLAIMS

Claims 9 and 16 form a first group.

Claims 10 and 13-15 form a second group.

Claims 11-12 should not be grouped together and should each be considered separately.

The reasons for these groupings are set forth in Appellants' arguments in Section VIII.

VIII. ARGUMENT

A. Claims 9-11 and 13-16 are not properly rejected under 35 U.S.C. §102(b) as being anticipated by Dennison

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference. M.P.E.P. §2131.

Dennison does not disclose "means for providing *an active region* on a substrate wherein the *active region comprises a plurality of discontinuous gate structures*" as recited in claim 9. The Examiner directs Appellant's attention to elements 12, 16, 20 and 24 in Figure 1 as disclosing the above-cited claim limitation. Paper No. 6, Page 2. Instead, Dennison discloses "providing a series of gate lines over a semiconductor substrate, the gate lines comprising memory array gate lines and peripheral circuitry gate lines, a *first gate line*

being positioned relative to a first peripheral area of the substrate for formation of a peripheral NMOS transistor, a *second gate line being positioned relative to a second peripheral area of the substrate* for formation of a peripheral PMOS transistor, a *third gate line being positioned relative to a memory array area of the substrate* for formation of a memory array NMOS transistor." Column 2, Lines 20-29. Further, Dennison discloses "a *first gate line 16 is positioned relative to a first peripheral area 18* of substrate 12 for formation of a peripheral NMOS transistor. A *second gate line 20 is positioned relative to a second peripheral area 22* of substrate 12 and n-well 14 for formation of a peripheral PMOS transistor. A *third gate line 24 is positioned relative to a memory array area 26* for formation of a memory array NMOS transistor." Column 3, Lines 19-25. Thus, Dennison discloses *three gate lines on **three** active regions* (gate line 16 on a first active region 18, gate line 20 on a second active region 22 and gate line 24 on a third active region 26). As stated in Appellant's response with a mailing date of May 14, 2002,

> *active regions are regions that are defined on the substrate via a LOCOS (Local Oxidation of Silicon) or similar process upon which gate stacks are formed. These active regions are separated by isolation regions that are typically formed by growing a thin field oxide region (FOX) between the active regions using a thermal oxidation process.* As a result, a plurality of active regions are formed on a single active region. Paper No. 7, Page 4.

Hence, Dennison does not disclose a single active region on a substrate comprising a plurality of discontinuous gate structures. Instead, Dennison discloses three active regions on the substrate. Nowhere does Dennison teach or even suggest that these active regions could all be sub-regions of an active region. Thus, Dennison does not disclose all the limitations of claim 9, and thus Dennison does not anticipate claim 9. M.P.E.P. §2131.

In response to Appellant's argument presented in Paper No. 7, the Examiner states that "*it is submitted that claims as written do not exclude the possibility that the active region have sub-regions. Note that the claims are given the broadest reasonable interpretation consistent with the specification during patent examination.* See In re Morris, 127 F.3d

1048, 44 USPQ2d 1023 (Fed. Cir. 1997)." Paper No. 8, Page 3. Appellant respectfully points out to the Examiner that the Examiner is entitled to give claim limitations their broadest reasonable interpretation *in light of the specification*. *In re Morris*, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997); M.P.E.P. §2111-§2116.01. The Examiner cannot transmogrify the meaning of a claim in order to find a reference to reject the claim. In particular, the *Examiner may not simply ignore language in the* claims. *All words in a claim must be considered in judging the patentability of that claim against the prior art*. *In re Wilson*, 424 F.2d 1382, 1385, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970); M.P.E.P. §2143.03. The claim states *an active region* that comprises a plurality of discontinuous gate structures which is supported at least in part on page 5, line 16 to page 6, line 10 and Figures 4-5 of Appellant's Specification. Thus, Dennison does not disclose all the limitations of claim 9, and thus Dennison does not anticipate claim 9. M.P.E.P. §2131.

Dennison does not disclose "means for *masking the plurality of gate structures* prior to the ion implantation" as recited in claim 10. The Examiner directs Appellant's attention to element 38 as the masking layer over the plurality of gate structures. Paper No. 6, Page 2. Further, as stated above, the Examiner asserts that the plurality of gate structures corresponds to elements 16, 20 and 24. Paper No. 6, Page 4. Instead, Dennison discloses that "referring to FIG. 2 a *photoresist masking layer 38* is *provided over second gate line 20, second peripheral PMOS substrate area 22, third gate line 24, and memory array NMOS substrate area 26*. An n-type *LDD implant 42*, preferably As, is then *provided into the exposed first peripheral NMOS substrate area 18 adjacent first gate line 16*." Column 3, Lines 36-41. Hence, Dennison discloses providing a photoresist masking layer only over two of the three gate lines (gate lines 20 and 24 and not gate line 16). Further, Dennison discloses implanting an LDD implant into the exposed substrate area 18. Thus, using the Examiner's definition of a plurality of gate structures corresponding to gate lines 16, 20 and 24, Dennison does not disclose a photoresist masking layer over the plurality of gate

structures prior to the ion implantation but only over a portion of the plurality of gate structures. Thus, Dennison does not disclose all the limitations of claim 10, and thus Dennison does not anticipate claim 10. M.P.E.P. §2131.

Dennison does not disclose "wherein *the active region comprises three gate structures*" as recited in claim 11. The Examiner directs Appellant's attention to elements 12, 16, 20 and 24 in Figure 1 as disclosing the above-cited claim limitation. Paper No. 6, Page 2. Instead, as stated above, Dennison discloses *three gate lines on* ***three*** *active regions* (gate line 16 on a first active region 18, gate line 20 on a second active region 22 and gate line 24 on a third active region 26). As stated above, *active regions are regions that are defined on the substrate via a LOCOS (Local Oxidation of Silicon) or similar process upon which gate stacks are formed. These active regions are separated by isolation regions that are typically formed by growing a thin field oxide region (FOX) between the active regions using a thermal oxidation process.* Hence, Dennison does not disclose a single active region on a substrate comprising a plurality of gate structures. Instead, Dennison discloses three active regions on the substrate. Thus, Dennison does not disclose all the limitations of claim 11, and thus Dennison does not anticipate claim 11. M.P.E.P. §2131.

As a result of the foregoing, Appellant respectfully asserts that not each and every claim limitation was found within Dennison and thus claims 9-11 and 13-16 are not anticipated by Dennison.

It is noted that words are italicized only for emphasis. Words that are italicized are not meant to imply that only those words are not disclosed in the cited prior art.

B. Claim 12 is not properly rejected under 35 U.S.C. §103(a) as being unpatentable over Dennison

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142. The motivation or suggestion to combine references must come from one of three possible sources: the nature of the problem to be solved, the teaching of the prior art and the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 47 U.S.P.Q.2d. 1453,1458 (Fed. Cir. 1998). The showings must be clear and particular. *In re* Lee, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 200); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

In order to reject under 35 U.S.C. §103, therefore, the Examiner must provide a proper motivation for combining or modifying the references. *In re Rouffet*, 47 U.S.P.Q.2d. 1453, 1457-1458 (Fed. Cir. 1998); M.P.E.P. §2142. The Examiner's motivation for modifying Dennison to provide an active region on a substrate comprising three gate structures where each of the three gate structures comprises a channel length of at least 0.13 μm disposed at least 0.2μm apart is "*because it would have been obvious to one ordinary skill in the art of making semiconductor devices to determine the workable or optimal range for the channel length and separated distance through routine experimentation and optimization to obtain optimal or desired device performance.*" Paper No. 6, Page 3.

The Examiner has not presented a *prima facie* case of obviousness for rejecting Dennison. The Examiner has not shown why Dennison should be modified to provide *an*

active region on a substrate comprising three gate structures from either the nature of the problem *to be solved, the teaching of the prior art and the knowledge of persons of ordinary skill in the art. In re Rouffet*, 47 U.S.P.Q.2d. 1453,1458 (Fed. Cir. 1998). Further, the Examiner has not shown why Dennison should be modified to provide an active region on a substrate comprising three gate structures *where each of the three gate structures comprises a channel length of at least 0.13 μm disposed at least 0.2μm apart from either the nature of the problem to be solved, the teaching of the prior art and the knowledge of persons of ordinary skill in the art. Id.* The Examiner must submit **objective evidence** and not rely on his subjective opinion in support of modifying Dennison to provide an active region on a substrate comprising three gate structures where each of the three gate structures comprises a channel length of at least 0.13 μm disposed at least 0.2μm apart. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). The Examiner simply states that one of ordinary skill of making semiconductor devices would determine the workable or optimal range for the channel length and separated distance through routine experimentation and optimization to obtain optimal or desired device performance. The Examiner has not presented any evidence for supporting the proposition that one of ordinary skill in the art would determine to modify Dennison to provide an active region on a substrate comprising three gate structures where each of the three gate structures comprises a channel length of at least 0.13 μm disposed at least 0.2μm apart simply from experimentation. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 12. Accordingly, one skilled in the art would not be able to recreate claim 12 in view of the cited prior art.

As a result of the foregoing, Appellants respectfully assert that the Examiner's *prima facie* case of obviousness is not taught or suggested by the cited prior art since there are numerous claim limitations not taught or suggested in the cited prior art, and thus one skilled in the art would not have been able to recreate claim 12 in view of the cited prior art.

IX. CONCLUSION

For the reasons noted above, the rejections of claims 9-16 are in error. Appellant respectfully requests reversal of the rejections and allowance of claims 9-16.

Respectfully submitted,

WINSTEAD SECHREST & MINICK P.C.

Attorneys for Appellant

By: _____

Robert A. Voigt, Jr.
Reg. No. 47,159
Barry S. Newberger
Reg. No. 41,527
Kelly K. Kordzik
Reg. No. 36,571

5400 Renaissance Tower
1201 Elm Street
Dallas, Texas 75270-2199
(512) 370-2832

APPENDIX

9. A system for forming a channel device comprising:

means for providing an active region on a substrate wherein the active region comprises a plurality of discontinuous gate structures; and

means for providing an ion implantation in the substrate.

10. The system of claim 9 wherein means for providing the ion implantation further comprises:

means for masking the plurality of gate structures prior to the ion implantation.

11. The system of claim 10 wherein the active region comprises three gate structures.

12. The method of claim 11 wherein each of the three gate structures comprises a channel length of at least 0.13μm disposed at least 0.2μm apart.

13. The system of claim 10 wherein the ion implantation comprises a lightly doped drain implant.

14. The system of claim 13 wherein the ion implantation further comprises a halo implant.

15. The system of claim 13 wherein the ion implantation further comprises a pocket implant.

16. The system of claim 9 wherein each of the plurality of discontinuous gate structures are connected to a gate voltage source.